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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **WATANABE, Kenichi et al.**

Group Art Unit: **2814**

Serial No.: **09/735,479**

Examiner: **PERALTA, Ginette**

Filed: **December 14, 2000**

P.T.O. Confirmation No.: **8362**

FOR: SEMICONDUCTOR DEVICE WITH DUAL DAMASCENE WIRING

RESPONSE TO THE RESTRICTION REQUIREMENT
DATED MAY 31, 2002

Commissioner for Patents
Washington, D.C. 20231

Date: June 13, 2002

Sir:

This paper is submitted in response to the Official Action dated **May 31, 2002**.

In the Action, restriction is required between Group (I), Claims 1-7, drawn to a semiconductor device; and Group (II), Claims 8-18, drawn to a method of manufacturing a semiconductor device.

Applicants hereby elect the subject matter of Group (I), Claims 1-7 for prosecution in this application. This election is made without traverse, it being understood that the applicants' rights to the filing of a divisional application directed to the non-elected subject matter under 35 USC 120 and 35 USC 121 are retained.

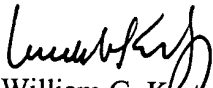
In the event that this paper is not timely filed, applicants hereby petition for an appropriate extension of time. The fee for any such extension may be charged to our Deposit Account No. 01-2340.

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In the event any additional fees are required in connection with this response, please charge our Deposit Account No. 01-2340.

Respectfully Submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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PATENT TRADEMARK OFFICE